UNITED STATES PATENT APPLICATION

OF

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FOR

ARRAY SUBSTRATE FOR IPS MODE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

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[0001] This application claims the benefit of Korean Patent Application No. 2000-79356, filed on December 20, 2000 in Korea, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) device, and more particularly to an array substrate and a fabricating method thereof for a liquid crystal display device that implements In-Plane Switching (IPS) in which an electric field applied to liquid crystal is generated in a plane parallel to a substrate.

Discussion of the Related Art

[0003] Until recently, a cathode-ray tube (CRT) has usually been used for displays. However, flat panel displays are becoming more common because of their small depth, low weight and low power consumption. Thin film transistor liquid crystal displays (TFT-LCDs) are currently undergoing development to improve their resolution and to reduce their thickness.

[0004] Generally, a liquid crystal display device includes an upper substrate and a lower substrate each having an electrode thereon and liquid crystal interposed therebetween. If the liquid crystal is aligned by an electric field generated by a voltage applied to the electrodes, desired images can be displayed by a change of transmissivity that depends on the alignment direction of the liquid crystal molecules.

[0005] The general structure of a conventional liquid crystal display device will be described hereinafter with reference to FIG. 1. FIG. 1 is a cross-sectional view

illustrating a structure of the conventional liquid crystal display device. As shown in the figure, a gate electrode 21 made of conductive material such as a metal is formed on a lower substrate 10, i.e., an array substrate. A gate insulating layer 30 including inorganic insulating material such as silicon oxide (SiO_2) or silicon nitride (SiN_X) is formed on the gate electrode 21 and on the lower substrate 10. An active layer 41 is formed on the gate insulating layer 30 using amorphous silicon. An ohmic contact layer 51, 52 is formed on the active layer 41 using a doped amorphous silicon. Source and drain electrodes 61, 62 made of conductive material are formed on the ohmic contact layer 51,52 respectively. The gate electrode, the source electrode and the drain electrode constitute a thin film transistor "T". A passivation layer 70 is then formed on the source and drain electrode 61,62 using inorganic insulating material or organic insulating material. A contact hole 71 through the passivation layer 70 exposes the drain electrode 62 to the air. A pixel electrode 81 made of transparent conductive material is formed on the passivation layer 70. The pixel electrode 81 contacts the drain electrode 62 through the contact hole 71. A black matrix 91 is formed beneath a part of an upper substrate 90 corresponding to the thin film transistor "T". A color filter 92 is formed beneath the black matrix 91. The color filter 92 has sub-color filters Red (R), Green (G) and Blue (B) arranged in a repeated order of R, G, B. A common electrode 93 made of transparent conductive material is formed beneath the color filter 92. In addition, a liquid crystal layer 100 is interposed between the upper and lower substrates 90, 10.

[0006] Liquid crystal molecules are aligned by an electric field generated perpendicularly to the substrates by a voltage applied to the pixel and common

electrodes in the conventional liquid crystal display device. Characteristics such as a transmissivity and an aperture ratio are good in the conventional liquid crystal display device and, because the common electrode serves as a ground, destruction of a liquid crystal cell caused by static electricity can be prevented. However, the conventional liquid crystal display device has disadvantages such as a narrow viewing angle. Accordingly, an in-plane switching (IPS) mode liquid crystal display device has been suggested as an alternative to overcome the disadvantages such as a narrow viewing angle.

SUMMARY OF THE INVENTION

[0007] Accordingly, the present invention is directed to an array substrate of in-plane switching (IPS) mode liquid crystal display device and a method for fabricating the same that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0008] An advantage of the present invention is to provide an in-plane switching liquid crystal display device that can improve a viewing angle and a production yield.

[0009] Another advantage of the present invention is to provide a fabricating method for an in-plane switching liquid crystal display device.

[0010] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0011] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an in-plane switching liquid crystal display device includes first and second substrates, a gate line and a data line defining a pixel region on the first substrate, a first line on the first substrate, a common line on the first line, a thin film transistor at a crossing portion between the gate and data lines, a plurality of pixel electrodes on the first substrate, a plurality of common electrodes on the first substrate, a first pixel electrode connecting line on the first substrate, and a liquid crystal layer between the first and second substrates. The first pixel electrode connecting line is partially overlapped with the common line. The in-plane switching liquid crystal display device further includes an auxiliary pattern extended from the first line. The auxiliary pattern is between the first line and the first pixel electrode connecting line. The auxiliary pattern is formed outermost of the common electrode. The in-plane switching liquid crystal display device further comprises a second line underneath the gate line. The thin film transistor includes gate, source and drain electrodes. The common electrode is at the same layer as the gate electrode. The pixel electrode is at the same layer as the source and drain electrodes.

[0012] In another aspect, an in-plane switching liquid crystal display device includes first and second substrates, a gate line and a data line defining a pixel region on the first substrate, a first line on the first substrate, a common line on the first line, a thin film transistor at a crossing portion between the gate and data lines, a plurality of pixel electrodes on the first substrate, a plurality of common electrodes on the first substrate, an auxiliary pattern extended from the first line, and a liquid crystal layer between the

first and second substrates. The in-plane switching liquid crystal display device further comprises a first pixel electrode connecting line on the first substrate. The first pixel electrode connecting line is partially overlapped with the common line. The auxiliary pattern is between the first line and the first pixel electrode connecting line. The auxiliary pattern is formed outermost of the common electrode. The in-plane switching liquid crystal display device further includes a second line underneath the gate line. The thin film transistor includes gate, source and drain electrodes. The common electrode is at the same layer as the gate electrode. The pixel electrode is at the same layer as the source and drain electrodes.

[0013] In another aspect, a method for fabricating an in-plane switching liquid crystal display device comprises the steps of forming a gate line and a data line defining a pixel region on a first substrate, forming a first line on the first substrate, forming a common line on the first line, forming a thin film transistor at a crossing portion between the gate and data lines, forming a plurality of pixel electrodes on the first substrate, forming a plurality of common electrodes on the first substrate, forming a first pixel electrode connecting line on the first substrate and forming a liquid crystal layer between the first substrate and a second substrate facing the first substrate. The first pixel electrode connecting line is partially overlapped with the common line. The method for fabricating an in-plane switching liquid crystal display device further comprises the step of forming an auxiliary pattern extended from the first line. The auxiliary pattern is between the first line and the first pixel electrode connecting line. The auxiliary pattern is formed outermost of the common electrode. The method for fabricating an in-plane switching liquid crystal display device further includes the step

of forming a second line underneath the gate line. The thin film transistor includes gate, source and drain electrodes. The common electrode is at the same layer as the gate electrode. The pixel electrode is at the same layer as the source and drain electrodes.

[0014] The viewing angle can be improved by introducing the in-plane switching (IPS) mode liquid crystal display device where the common electrode and the pixel electrode are formed on the same substrate and the liquid crystal is aligned by lateral electric field generated by a voltage applied to the common and pixel electrodes. The auxiliary patterns are formed between the first pixel electrode connecting line and the data line parallel to the data line. When the pixel electrode and the data line are formed simultaneously in a same process, there may be residues of conductive material such as a metal. Accordingly, the auxiliary pattern step prevents residues from connecting the pixel electrode to the data line and thus prevents a short circuit.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0017] In the drawings:

[0018] FIG. 1 is a cross-sectional view illustrating a structure of a conventional liquid crystal display device;

[0019] FIG. 2 is a plan view illustrating a pixel of an array substrate according to a first embodiment of the present invention;

[0020] FIG. 3 is a cross-sectional view taken along III-III of FIG. 2;

[0021] FIGs. 4A to 4C are cross-sectional views illustrating fabricating sequences of an array substrate according to the present invention;

[0022] FIG. 5 is a cross-sectional view of a portion "A" of FIG. 2;

[0023] FIG. 6 is a plan view illustrating a pixel of an array substrate according to a second embodiment of the present invention; and

[0024] FIG. 7 is a cross-sectional view of a portion "B" of FIG. 6.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0025] Reference will now be made in detail to the illustrated embodiments of the present invention, which are illustrated in the accompanying drawings.

[0026] FIG. 2 is a plan view illustrating a pixel of an array substrate according to a first embodiment of the present invention and FIG. 3 is a cross-sectional view taken along III-III of FIG. 2. As shown in the figures, first and second lines 121, 122 made of metallic material having a low electric resistance are formed horizontally on a transparent insulating substrate 110. The first and second lines 121, 122 are for reducing the electric resistance of a common line 133 and a gate line 131, respectively. The common line 133 and the gate line 131 are formed on the first line 121 and the second line 122, respectively. A gate electrode 132 extending from the gate line 131 is

formed on the second line 122. First, second, third and fourth common electrodes 135, 136, 137, 138 are vertically arranged in the context of FIG. 2. Upper ends of the common electrodes are connected to the common line 133, and a common electrode connecting line 134 is connected to lower ends of the common electrodes 135, 136, 137, 138. A gate insulating layer 140 including inorganic insulating material such as silicon oxide (SiO_2) or silicon nitride (SiN_X), for example, is formed on the substrate 110. A semiconductor layer 151 including amorphous silicon is formed on a part of the gate insulating layer 140 corresponding to the gate electrode 132 and the semiconductor layer 151 serves as an active layer of a thin film transistor. Ohmic contact layers 161, 162 including doped amorphous silicon are formed on the semiconductor layer 151. The ohmic contact layers are for reducing an electric resistance caused by a contact between the semiconductor layer 151 and a source and drain electrodes 172, 173. A data line 171, the source electrode 172, the drain electrode 173, a first and second pixel electrode connecting lines 174, 175 and a first, second and third pixel electrodes are formed with conductive material such as a metal on the ohmic contact layer 161, 162. The data line 171 defines a pixel region by crossing the gate line 131. The source electrode 172 extends from the data line 171. The drain electrode 173 is spaced apart from the source electrode 172. The gate electrode and the source and drain electrode constitute the thin film transistor. The first, second and third pixel electrodes 176, 177 and 178 are vertically arranged in an alternating order with the corresponding common electrodes 135, 136, 137, 138. Upper and lower ends of the pixel electrodes are connected to the horizontal first and second pixel electrode connecting line 174, 175 respectively. The second pixel electrode connecting line 175 is connected to the drain

electrode 173. A passivation layer may further be formed on the data line 171 and the pixel electrodes 176, 177, 178.

[0027] The present invention can improve a viewing angle by forming the pixel and common electrode on the same substrate, and thus driving liquid crystal molecules by applying a lateral electric field to the liquid crystal. The lateral electric field is generated when a voltage is applied to the pixel and common electrodes.

[0028] A fabricating method for an array substrate for in-plane switching (IPS) mode liquid crystal display device will be described more in detail hereafter with reference to FIG. 2 and FIGs 4A to 4C. FIGs. 4A to 4C are cross-sectional views taken along III-III of FIG. 2 illustrating fabricating sequences of an array substrate according to the present invention.

[0029] Referring to FIG. 2 and FIG. 4A, horizontal first and second lines 121, 122 are formed on the transparent insulating substrate 110 by depositing and patterning conductive material such as a metal. The first and second lines 121, 122 are formed desirably with material having a good adhesive property and a low electric resistance. Then a gate line 131, a gate electrode 132, a common line 133, a common electrode connecting line 134, and first, second, third and fourth common electrodes 135, 136, 137, 138 are formed by depositing and patterning conductive material such as a metal. The common line 133 and the gate line 131 are formed on the first and second lines 121, 122, respectively.

[0030] Referring to FIG. 2 and FIG. 4B, a gate insulating layer 140 covering the gate electrode 132 is formed on the substrate 110. A semiconductor layer 151 and a doped

semiconductor layer 163 are formed over the gate electrode 132 by depositing and patterning amorphous silicon and doped amorphous silicon respectively.

[0031] Referring to FIG. 2 and FIG. 4C, a data line 171, a source electrode 172, a drain electrode 173, first and second pixel electrode connecting lines 174, 175, and first, second and third pixel electrodes 176, 177, 178 are formed by depositing and patterning conductive metallic material such as molybdenum (Mo) or chromium (Cr), for example. The ohmic contact layers 161, 162 is subsequently formed by removing the doped semiconductor layer between the source electrode 172 and the drain electrode 173.

[0032] As described above, the first and second lines 121, 122 that are formed under the common line 133 and the gate line 131, respectively, to reduce the electric resistances prevent signals from being delayed. Because the pixel electrode and the common electrode are formed on the same substrate, and the pixel electrode and the data line are formed simultaneously in the same process, the fabricating process can be simplified according to the present invention. However, when the data line and the pixel electrodes are formed by etching the metallic material, a short circuit may occur because of residue of the metallic material between the data line 171 and the first pixel electrode connecting line 174.

[0033] FIG. 5 is a cross-sectional view of a portion "A" of FIG. 2. As shown in the figure, a step is formed between the data line 171 and the first pixel electrode connecting line 174 by the first line 121. The common line 133 is formed on the substrate 110 and the gate insulating layer 140 is formed on the common line 133. The data line 171 and the first pixel electrode connecting line 174 are formed on the gate insulating layer 140. The data line 171 and the first pixel electrode connecting line 174

are formed simultaneously in the same process. After the metallic material between the data line 171 and the first pixel electrode connecting line 174 are etched away during the forming process for the data line 171 and the first pixel electrode connecting line 174, there may exist residues 200 due to a step generated by the first line 121. The residues 200 may electrically connect the data line 171 to the first pixel electrode connecting line 174 and thus cause a short.

[0034] A second embodiment of the present invention to overcome the short problem will be described hereinafter with reference to FIG. 6 and FIG. 7. FIG. 6 is a plan view illustrating a pixel of an array substrate according to a second embodiment of the present invention and FIG. 7 is a cross-sectional view of a portion "B" of FIG. 6. The structure of the array substrate of the second embodiment is same as that of the first embodiment except portions of first and fourth common electrodes. As shown in FIG. 7, auxiliary patterns 191, 192 are vertically extended under the first and fourth common electrodes 135, 138 disposed between the data line 171 and the first pixel electrode connecting line 174. Accordingly as shown in FIG. 7, steps are formed perpendicularly to the steps generated by the first line between the data line 171 and the first pixel electrode connecting line 174. The steps generated by the auxiliary patterns 191, 192 prevent residues from connecting the data line 171 to the first pixel electrode connecting line 174 and thus prevent a short circuit.

[0035] It will be apparent to those skilled in the art that various modifications and variation can be made in the fabrication and application of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the

present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.